wherein said video signal is constituted by bit blocks having a plurality of attributes and wherein said driver ICs are controlled by using said bit blocks.

REMARKS

Claims 1-16 are pending in this application; and in the Office Action, the Examiner rejected claims 1-8 and 10-16 over the prior art, principally U.S. Patent 5,801,674 (Shimizu), and rejected Claim 9 under 35 U.S.C. §112, first paragraph. Also, the Examiner objected to Figures 13 and 20, and noted several objections to the specification.

More specifically, Claims 1 and 2 were rejected under 35 U.S.C. §103 as being unpatentable over Shimizu in view of U.S. Patent 5,751,261 (Zavracky, et al.), Claims 3, 6 and 7 were rejected under 35 U.S.C. §103 as being unpatentable over Shimizu in view of Zavracky and U.S. Patent 5,623,519 (Babcock, et al.), and Claims 4 and 5 were rejected under 35 U.S.C. §102 as being fully anticipated by Shimizu. Also, Claim 8 was rejected under 35 U.S.C. §103 as being unpatentable over Shimizu in view of Zavracky, Babcock and U.S. Patent 5,974,464 (Shin, et al.), and Claims 10-16 were rejected under 35 U.S.C. §103 as being unpatentable over Shimizu in view of Babcock. Claim 9, it may be noted, was not rejected over the prior art.

This opportunity is being taken to amend the specification and the drawings to address several objections raised by the Examiner, and to amend independent Claims 1, 4, 6, 10, 12 and 14 to emphasize differences between the claims and the prior art.

With regard to the drawings, Applicants herein request that Figure 20 be labeled "Prior art," and that Figure 13 be amended to show "(a)" and "(b)" in the appropriate locations. The changes to Figures 13 and 20 are shown in the sketches submitted herewith. In view of these changes to Figures 13 and 20, the Examiner is asked to reconsider and to withdraw the objections to the drawings.

With respect to the specification, the Examiner objected to the use of various abbreviations, such as LSI, TFT and PC. These abbreviations are well understood in the art. For instance, PC, as is very well known, stands for "personal computer," and WOA stands for "wiring on array." Because these abbreviations are so well known, it is not necessary to amend the specification to elaborate on these terms. The specification is being amended, though, to add references to various Figure numbers to facilitate reading the description, and to "A" and "B" on page 19, line 23 from upper case to lower case.

In light of the above comments and the changes requested herein to the specification, the Examiner is respectfully asked to reconsider and to withdraw the objections to the specification.

With respect to the rejection of Claim 9 under 35 U.S.C. §112, Applicants note that this claim is directed to the use of a dummy circuit in an upstream driver IC. This feature is discussed in the specification, on page 5, lines 27-31. As explained there, the purpose of the "dummy circuit" is to allow substantial matching, within a permissible range, of video and clock phases, without a phase locked loop circuit. In view of this explanation and disclosure, one of ordinary skill in the art would be able to practice the subject matter of claim 9, and the Examiner is, thus, requested to reconsider and to withdraw the rejection of Claim 9 under 35 U.S.C. §112.

With regard to the rejection of the claims over the prior art, Applicants note that there is an important feature of this invention that is not shown or suggested in the prior art. In particular, with the present invention, the ICs of the driver are connected in series, for example via signal lines, as illustrated in Figure 1. With the arrangement disclosed in Shimizu, in contrast, the drivers are not connected in series via the signal lines. Instead, the drivers are connected in parallel to the signal lines.

Independent Claims 1, 4, 6, 10, 12 and 14 have been amended to emphasize this aspect of the invention. Specifically, Claims 1 and 4 are being amended to indicate expressly that the driver ICs are connected in series using signal lines or a video transmission line, and Claims 10, 12 and 14 are being amended to indicate that the video signal is transmitted in series to the driver ICs.

This feature of this invention is of utility because, as discussed in the present application, it reduces the number of required IC interconnects. This, in turn, facilitates manufacture of the LCD driver by the chip-on-glass wiring-on-array technique.

The other references of record have been reviewed, and they are believed to be no more relevant than Shimizu. For example, Zavracky, et al. was cited for its teaching of transferring a silicon substrate top a glass substrate, and Babcock, et al. was cited for disclosing the synchronization of a serial stream of data. None of the references, either individually or in combination, teaches the principal of connecting the driver ICs of an LCD device in series in the manner described in Claims 1, 4, 6, 10, 12 and 14.

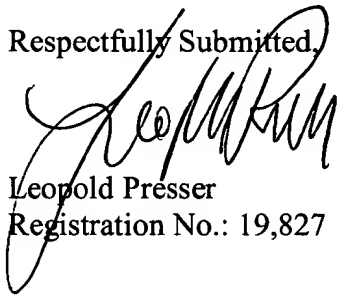
Accordingly, Claims 1, 4, 6, 10, 12 and 14 patentably distinguish over the prior art and are allowable. Claims 2 and 3 are dependent from Claim 1 and are allowable therewith, Claim 5 is dependent from Claim 4 and is allowable therewith, and Claims 7-9 are dependent from Claim 6 and are allowable therewith. Similarly, Claims 11, 13, and 15 and 16 are dependent from Claims 10, 12 and 14, respectively, and are allowable therewith. The Examiner is, thus, respectfully requested to reconsider and to withdraw the above-discussed rejections of Claims 1-8 and 10-16 over the prior art, and to allow Claims 1-16.

Moreover, applicant also encloses a copy of a **"Version with Markings Showing Changes Made"**, indicative of the amendments which have been implemented to the present

application and to facilitate the Examiner's review thereof.

For the reasons advanced above, the Examiner is asked to reconsider and to withdraw the objections to the drawings and to the specification. The Examiner is also requested to reconsider and to withdraw the rejection of Claim 9 under 35 U.S.C. §112, to reconsider and to withdraw the rejections of Claims 1-8 and 10-16 over the prior art, and to allow Claims 1-16. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone John S. Sensny.

Respectfully Submitted,



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"VERSION WITH MARKINGS SHOWING CHANGES MADE"

IN THE DRAWINGS

Drawing Figures 13 and 20 have been amended marked in red ink.

IN THE SPECIFICATION

The specification has been amended as follows:

--(2) Command bit block 45

This is a bit block that is received in consonance with an arbitrary timing during the blanking period. The header 41, which represents a command bit block, is [1100]. Each source driver IC 20 (Fig. 1) interprets the control data contained in the data 42, and drives the liquid crystal cell 2. Example control data are as follows.

(a) Start of transmission for video data

[0000-0000-0000-0000-0000-0000]

This command is used to provide notification that video data transmission has begun. After this command is issued, the transmission of video data using a data bit block, which will be described later, is initiated.

(b) Start of transmission of gamma data

[1000-1000-1000-1000-1000-1000]

This command is used to provide notification that the transmission of gamma compensation data (value for generating a reference voltage) has begun. After this command is issued, the transmission of gamma data using a data bit block, which will be described later, is initiated.

(c) Strobe ON/OFF

Strobe ON [1101-1101-1101-1101-1101-1101]

Strobe OFF [1100-1100-1100-1100-1100-1100]

These commands are used to provide notification that output to the liquid crystal cell 2 (Fig. 1) has begun. Upon the receipt of the command strobe ON, the driver controller 29 sets a strobe (STB) signal, which is to be transmitted to the LCD source driver 31, High. While upon the receipt of the command strobe OFF, the driver controller 29 sets a strobe (STB) signal, which is to be transmitted to the LCD source driver 31, Low. Thus, during a period wherein the strobe signal is High, the output to the liquid crystal cell 2 can be maintained in a high impedance state.

(d) Designation of output polarity

Positive polarity output [1111-1111-1111-1111-1111-1111]

Negative polarity output [1110-1110-1110-1110-1110-1110]

These commands are used to designate the polarity of a voltage output to the liquid crystal cell 2. Upon the receipt of one of these commands, the driver controller 29 (Fig. 3) will set or reset an internal polarity control signal (POL).

(3) Data bit block 46

This is a bit block used for the transmission of video data or of gamma compensation data. The header 41 is [1110] and represents a data bit block, while the contents of the block are identified by using a command that was previously transmitted.

(a) Video data [Red 8-bit] [Green 8-bit] [Blue 8-bit]

The video data for one line are transmitted sequentially. For the XGA, 1024 data bit blocks 46 are sequentially received. The driver 29 for each source driver IC 20 (Fig. 1) receives only its own, individual data, and while it does this, it replaces the data bit block 46 with a wait bit block

(which will be described later), and transmits the wait bit block to the succeeding source driver IC 20.

(b) Gamma compensation data [Gamma 10-bit][00000000000000]

This is a case where a reference gamma compensation voltage having a 10-bit precision is generated, for the gamma compensation the required number of data sets are transmitted. The drivers 29 of all the source driver ICs 20 may either receive the same data, or may receive different data.

(4) Wait bit block 47

This is used only by the source driver ICs 20 (Fig. 1). The header 41 is [1111] (wait) and represents a wait bit block. During the reception of video data, each source driver IC 20 transmits a wait bit block 47 to a succeeding source driver IC 20. During the reception of the wait bit block 47, the source driver IC 20 does not perform any process, and waits to receive the video data that is included in the data bit block 46.

Fig. 5B is a diagram showing the transmission of n-line video data by using the input of a first chip that is the first source driver IC 20 and the input of a second chip that is the next source driver IC 20. After the blanking period (Sync: synchronization period), the video data transmission start command in the command bit block 45 is received, and then video data for one line is received. Subsequently, the strobe ON command is received at an appropriate time. At this time, the source driver IC 20 starts writing data to the liquid crystal cell 2 (Fig. 1). Actually, a voltage is applied to the liquid crystal cell 2 when the strobe OFF command is next received, and until that time, the output is maintained in a high impedance state. Positive output is

selected by the output polarity designation command that is issued between the strobe ON command and the strobe OFF command. During the reception of its own, individual video data, the first chip in the upper portion in Fig. 5B transmits the wait bit block 47 to a succeeding source driver IC 20 (a second chip). The second chip in the lower portion skips the wait bit block 47, starts reception of the video data, and writes data to the liquid crystal cell 2.

Figs. [13A] 13a and [13B] 13b are diagrams showing the process for generating a control signal (waveforms and the shifting of the state of each control signal). In Fig. 13A, latch 82 represents the output of the latch 82 in Fig. 12, and the latches 85 and 86 represent the video data that are latched and that, via the switch 83, are output to the LCD source driver 31. As is shown in Fig. 13B, when the first video data is received following the issue of the video data transmission start command (Cmd Video), the one pulse signal SPin is output. That is, the state is shifted from 0 to 1. Also, the signal STB is set to 1 upon the receipt of a strobe ON command (Cmd StbOn), and is cleared upon the receipt of a strobe OFF command (Cmd StbOf). In addition, upon the receipt of the output polarity designation command (Cmd Pos/Cmd Neg), the signal POL is shifted to a bit that represents the designated polarity. In this embodiment, the controller 88 is operated at 1/28 of the input clock.

IN THE CLAIMS

Claims 1, 4, 6, 10, 12 and 14 have been amended as follows:

--1. (Once Amended) A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and a driver for applying a voltage to said liquid crystal cell based on an input video signal, wherein said driver includes a plurality of driver ICs that are mounted on said substrate and are cascade-connected in series using signal lines.

4. (Once Amended) A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and

a driver for distributing an input video signal to a plurality of [chain-connected] driver ICs chain-connected in series using signal lines, and for applying a voltage to said liquid crystal cell by employing said driver ICs,

wherein said driver distributes said video signal to said plurality of driver ICs with providing a masking signal from an upstream driver IC to a downstream driver IC of said plurality of driver ICs, wherein said masking signal masks said video signal to be provided by said upstream driver IC.

6. (Once Amended) A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and

a driver for distributing an input video signal to a plurality of driver ICs that are cascade-connected, and for applying a voltage to said liquid crystal cell by employing said driver ICs,

wherein said plurality of driver ICs of said driver are cascade-connected in series by a video transmission line provided on said substrate, and are controlled by serial data that are transmitted along said video transmission line.

10. (Once Amended) A liquid crystal controller comprising:

a receiver for receiving a video signal from a host to display an image;

a sequencer for, upon the receipt of a control signal from said host, generating header information for packet data that are to be output to an LCD driver comprising a plurality of driver ICs which are cascade-connected in series; and

output means for converting said video signal received from said receiver into a serial video signal, for adding said header information generated by said sequencer to said serial video signal, and for outputting the resultant serial video signal to the ICs of said LCD driver.

12. (Once Amended) A video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs, comprising the steps of:

transmitting a video signal, including a horizontal blanking period, to said driver ICs in series via a serial interface; and

transmitting a synchronization pattern during said horizontal blanking period in order to synchronize said video signal for said driver ICs.

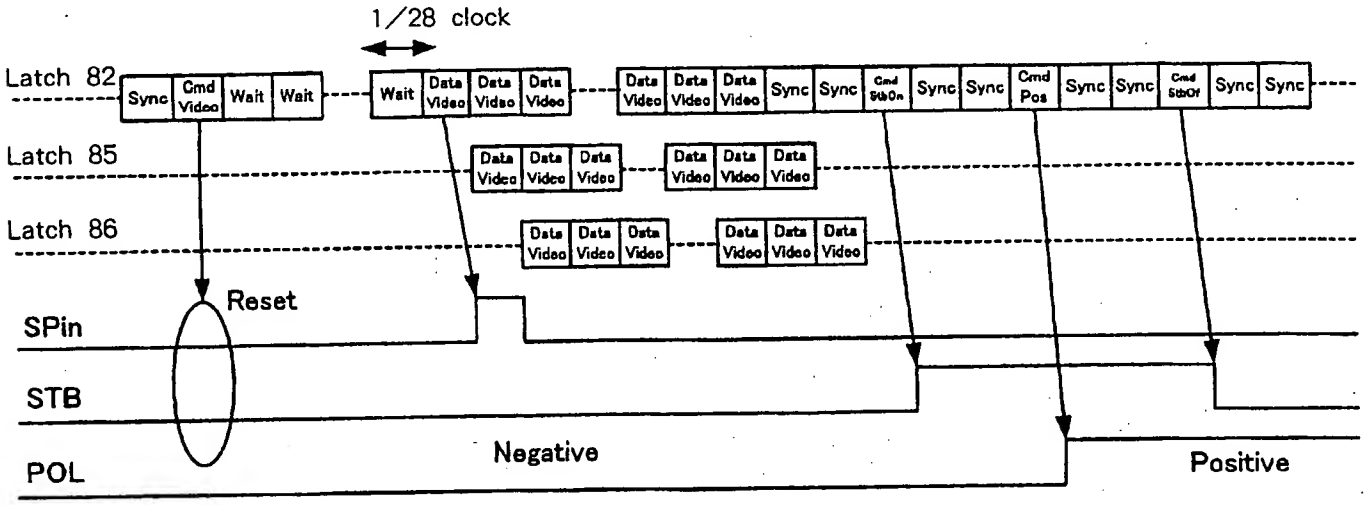
14. (Once Amended) A video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs that are cascade-connected, comprising the steps of:

transmitting a video signal via a serial interface to said driver ICs that are cascade-connected in series; and

applying to an LCD a voltage based on said video signal that is received and that is to be processed by each of said driver ICs;

wherein said video signal is constituted by bit blocks having a plurality of attributes and wherein said driver ICs are controlled by using said bit blocks.

(a)



(b)

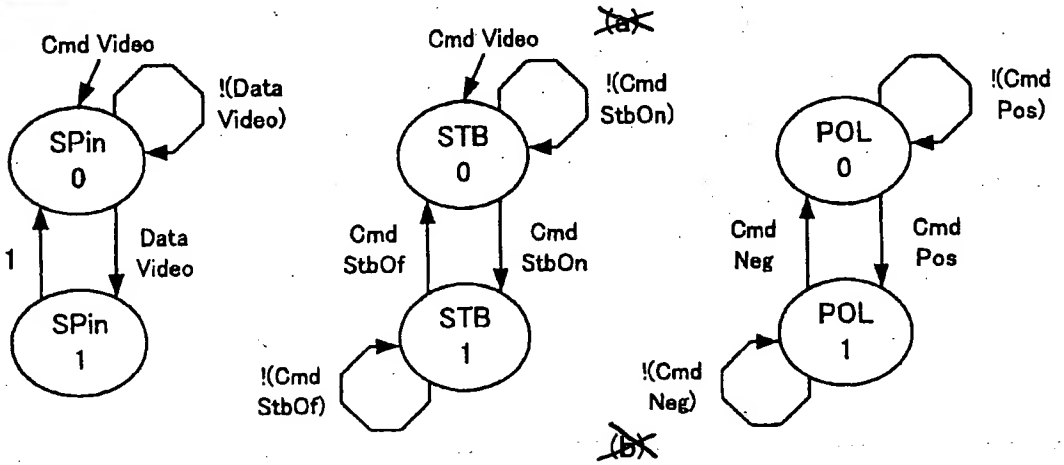


Fig. 13

Prior Art

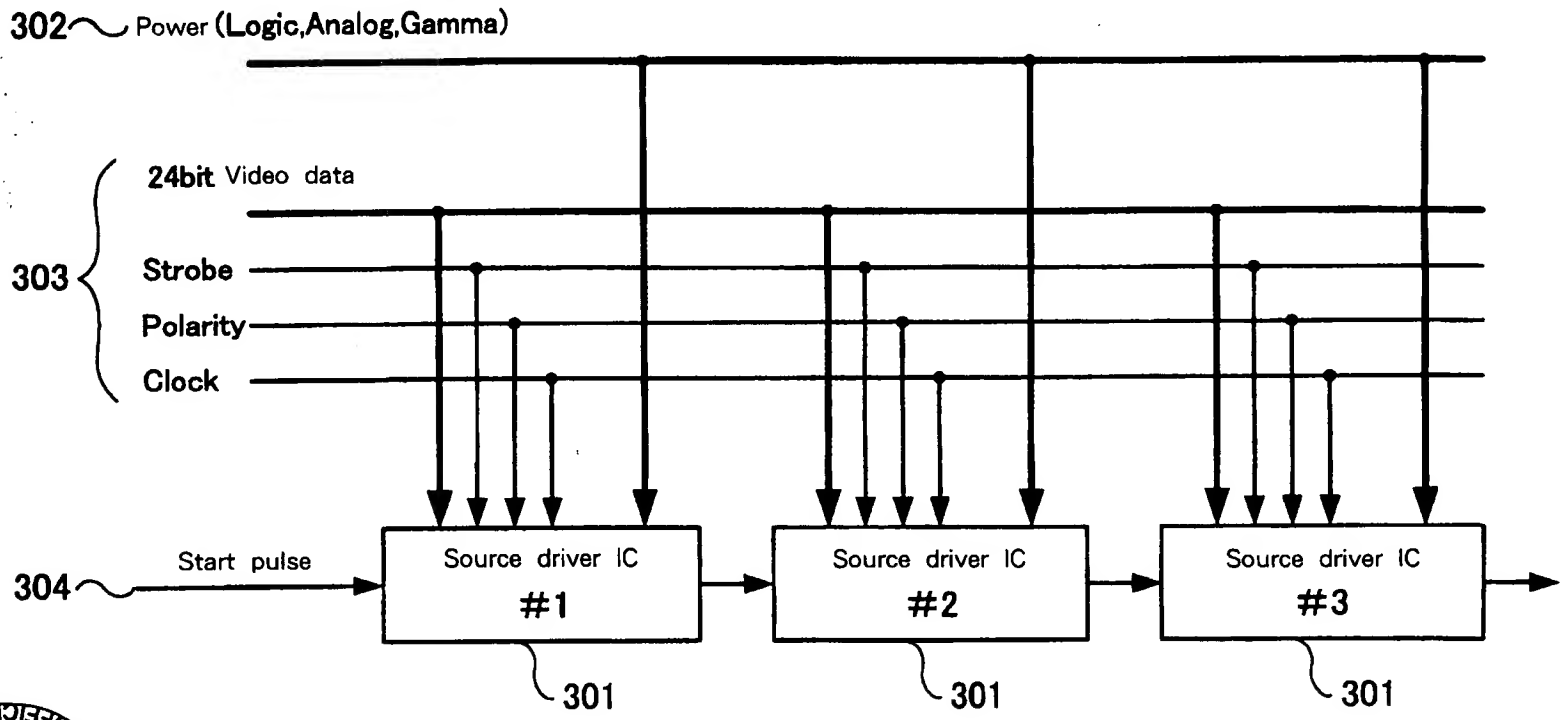


Fig. 20